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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,456	08/30/2001	Gary L. Swoboda	TI-30478	9920

23494 7590 12/21/2005

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EXAMINER	
GUILL, RUSSELL L	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 12/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,456	SWOBODA, GARY L.	
	Examiner	Art Unit	
	Russell L. Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,13,16,17 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,13 and 25* is/are rejected.

7)☒ Claim(s) *4,5,16,17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to an Amendment filed October 20, 2005. Claims 1, 4, 5, 13, 16, 17 and 25 have been amended. Claims 2, 3, 6 - 12, 14, 15, 18 - 24, 26 and 27 are canceled. Claims 1, 4, 5, 13, 16, 17 and 25 are pending. Claims 1, 4, 5, 13, 16, 17 and 25 have been examined. Claims 1, 13 and 25 have been rejected. Claims 4, 5, 16 and 17 are objected to.

Response to Remarks

2. **Regarding claims 1, 13 and 25** rejected under 35 USC § 103:

   2.1. Applicant's arguments with respect to claims 1, 13 and 25 have been considered but are moot in view of the new ground(s) of rejection caused by Applicant's amendments.

3. **Regarding claims 5 and 17** rejected under 35 USC § 103:

   3.1. Applicant's arguments with respect to claims 5 and 17 have been fully considered and are persuasive. The rejections are withdrawn.

4. **Regarding claims 4 and 16** rejected under 35 USC § 103:

   4.1. Applicant's arguments with respect to claims 4 and 16 have been fully considered and are persuasive. The rejections are withdrawn.

Claim Objections

5. **Claim 4** is objected to because of the following informalities: The claim depends from a canceled claim 3. For the purpose of claim examination, the claim is interpreted as depending from claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. **Claims 1, 13 and 25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards065 (U.S. Patent 6,918,065) in view of Edwards047 (U.S. Patent 6,530,047), further in view of admitted prior art by the Applicant.

8.1. Regarding claim 1, Edwards065 teaches:

8.1.1. A method of exporting from a data processor emulation information (**column 2, lines 9 - 15; and column 4, lines 5 - 15; and column 6, lines 1 - 15; and figure 1; and column 7, lines 45 - 50**) including emulation control information and emulation data (**figure 7; and Table 1; and Table 2; and Table 3; and Table 4**), comprising:

8.1.2. arranging the emulation information into information blocks (**figure 7; and Table 1; and Table 2; and Table 3; and Table 4**);

8.1.3. outputting a sequence of the information blocks from the data processor (**figure 8; and column 2, lines 10 - 67**); and

8.1.4. said arranging step including providing some of the information blocks of the sequence with relative proportions of emulation control information and emulation data that differ from the relative proportions of emulation control information and emulation data in other blocks of

the sequence (**figure 8, elements 811, 812A, 812B, 813; and Table 1; and Table 2; and Table 3; and Table 4**).

8.2. **Regarding claim 1**, Edwards065 does not specifically teach:

8.2.1. arranging the emulation information into ***fixed length*** information blocks.

8.2.2. outputting a sequence of the information blocks from the data processor ***via a plurality of terminals of the data processor.***

8.3. **Regarding claim 1**, Edwards047 teaches:

8.3.1. outputting a sequence of the information blocks from the data processor via a plurality of terminals of the data processor (**figure 1, element 107; and figure 4; and figure 5; and column 7, lines 49 - 57**).

8.4. **Regarding claim 1**, admitted prior art provided by the Applicant teaches:

8.4.1. arranging the emulation information into ***fixed length*** information blocks (**figure 20 of the Applicant's drawings**).

8.5. The motivation to use the art of Edwards047 with the art of Edwards065 would have been the benefit recited in Edwards047 that the widths of the link between the integrated circuit and the external system could be increased to meet debugging bandwidth needs of different applications (**column 7, lines 49 - 57**). Further, the same inventor produced both inventions.

8.6. The motivation to use the admitted prior art of the Applicant with the art of Edwards065 would have been the knowledge of the ordinary artisan that a design using fixed length blocks is faster to implement than a variable length block design.

8.7. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Edwards047 with the art of Edwards065 to produce the claimed invention.

8.8. **Regarding claim 13**, Edwards065 teaches:

8.8.1. An integrated circuit device (**figure 1, element 101**), comprising:

8.8.2. a data processing portion for performing data processing operations (**figure 1, element 102**);

8.8.3. an emulation information collector coupled to said data processing portion for receiving emulation data therefrom (**figure 1, elements 102, 103, 104**), said collector operable for arranging the emulation data and associated emulation control information into information blocks (**figure 1, element 103; figure 7; and Table 1; and Table 2; and Table 3; and Table 4; and column 6, lines 1 - 15**);

8.8.4. a ***link*** coupled to said collector for permitting said collector to communicate with an ***external device*** located externally of said integrated circuit device (**figure 1, elements 103, 106, and unlabelled I/O link between elements 103 and 106; and column 6, lines 10 - 15**).

8.8.5. said collector operable for providing to said ***link*** a sequence of said information blocks to be output to the ***external device*** (**figure 7, figure 8, and column 6, lines 1 - 15**), said collector further operable for providing some of the information blocks of the sequence with relative proportions of emulation control information and emulation data that differ from the relative proportions of emulation control information and emulation data in other blocks of the sequence (**figure 8, elements 811, 812A, 812B, 813; and Table 1; and Table 2; and Table 3; and Table 4**).

8.9. **Regarding claim 13**, Edwards065 does not specifically teach:

8.9.1. an emulation information collector coupled to said data processing portion for receiving emulation data therefrom, said collector operable for arranging the emulation data and associated emulation control information into ***fixed length*** information blocks.

8.9.2. ***a plurality of terminals coupled to said collector*** for permitting said collector to communicate with an emulation controller located externally of said integrated circuit device.

8.9.3. ***a plurality of terminals coupled to said collector*** coupled to said collector for permitting said collector to communicate with an ***emulation controller*** located externally of said integrated circuit device.

8.9.4. said collector operable for providing to said ***terminals*** a sequence of said information blocks to be output to the ***emulation controller***, said collector further operable for providing some of the information blocks of the sequence with relative proportions of emulation control information and emulation data that differ from the relative proportions of emulation control information and emulation data in other blocks of the sequence.

8.10. **Regarding claim 13**, Edwards047 teaches:

8.10.1. *a plurality of terminals coupled to said collector* for permitting said collector to communicate with an emulation controller located externally of said integrated circuit device **(figure 1, elements 107, 106, 103; and figure 4; and figure 5; and column 7, lines 49 - 57)**.

8.10.2. *a plurality of terminals coupled to said collector* coupled to said collector for permitting said collector to communicate with an *emulation controller* located externally of said integrated circuit device **(figure 1, elements 107, 106, 103; and figure 4; and figure 5; and column 7, lines 49 - 57; and column 8, lines 10 - 20)**.

8.10.3. said collector operable for providing to said *terminals* a sequence of said information blocks to be output to the *emulation controller* **(figure 1, elements 107, 106, 103; and figure 4; and figure 5; and column 7, lines 49 - 57; and column 8, lines 10 - 20)**.

8.11. **Regarding claim 13**, admitted prior art provided by the Applicant teaches:

8.11.1. arranging the emulation data and associated emulation control information into *fixed length* information blocks **(figure 20 of the Applicant's drawings)**.

8.12. The motivation to use the art of Edwards047 with the art of Edwards065 would have been the benefit recited in Edwards047 that the widths of the link between the integrated circuit and the external system could be increased to meet debugging bandwidth needs of different applications **(column 7, lines 49 - 57)**. Further motivation would have been the benefit recited in Edwards047 that the external system is capable of stopping, starting and resetting the processor through the link **(column 3, lines 14 - 20)**. Further, the same inventor produced both inventions.

8.13. The motivation to use the admitted prior art of the Applicant with the art of Edwards065 would have been the knowledge of the ordinary artisan that a design using fixed length blocks is faster to implement than a variable length block design.

8.14. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Edwards047 with the art of Edwards065 to produce the claimed invention.

8.15. **Regarding claim 25**, Edwards065 teaches:

8.15.1. A data processing system (**figure 1**), comprising:

8.15.2. an integrated circuit (**figure 1, element 101**), including a data processing portion for performing data processing operations (**figure 1, element 102**);

8.15.3. an external device located externally of said integrated circuit and coupled to said integrated circuit (**figure 1, elements 103, 106, and unlabelled I/O link between elements 103 and 106**);

8.15.4. said integrated circuit including an emulation information collector coupled to said data processing portion for receiving emulation data therefrom (**figure 1, elements 102, 103, 104**), said collector operable for arranging the emulation data and associated emulation control information into information blocks (**figure 1, element 103; figure 7; and Table 1; and Table 2; and Table 3; and Table 4; and column 6, lines 1 - 15**); and

8.15.5. said collector coupled to said external device for permitting said collector to communicate with said external device (**figure 1, elements 103, 106, and unlabelled I/O link between elements 103 and 106; and column 6, lines 10 - 15**), said collector operable for outputting to said external device a sequence of said information blocks (**figure 7, figure 8, and column 6, lines 1 - 15**), said collector further operable for providing some of the information blocks with relative proportions of emulation control information and emulation data that differ from the relative proportions of emulation control information and emulation data in other blocks of the sequence (**figure 8, elements 811, 812A, 812B, 813; and Table 1; and Table 2; and Table 3; and Table 4**).

8.16. **Regarding claim 25**, Edwards065 does not specifically teach:

8.16.1. an ***emulation controller*** located externally of said integrated circuit and coupled to said integrated circuit ***for controlling emulation operations of said integrated circuit*** .

8.16.2. said integrated circuit including an emulation information collector coupled to said data processing portion for receiving emulation data therefrom, said collector operable for arranging the emulation data and associated emulation control information into ***fixed length*** information blocks.

8.16.3. said collector coupled to said *emulation controller* for permitting said collector to communicate with said *emulation controller*, said collector operable for outputting to said *emulation controller* a sequence of said information blocks, said collector further operable for providing some of the information blocks with relative proportions of emulation control information and emulation data that differ from the relative proportions of emulation control information and emulation data in other blocks of the sequence.

8.17. **Regarding claim 25**, Edwards047 teaches:

8.17.1. an *emulation controller* located externally of said integrated circuit and coupled to said integrated circuit *for controlling emulation operations of said integrated circuit* **(figure 1, elements 107, 106, 103; and figure 4; and figure 5; and column 7, lines 49 - 57; and column 8, lines 10 - 20).**

8.17.2. said collector coupled to said *emulation controller* for permitting said collector to communicate with said *emulation controller*, said collector operable for outputting to said *emulation controller* a sequence of said information blocks **(figure 1, elements 107, 106, 103; and figure 4; and figure 5; and column 7, lines 49 - 57; and column 8, lines 10 - 20).**

8.18. **Regarding claim 25**, admitted prior art provided by the Applicant teaches:

8.18.1. arranging the emulation data and associated emulation control information into *fixed length* information blocks **(figure 20 of the Applicant's drawings).**

8.19. The motivation to use the art of Edwards047 and the admitted prior art of the Applicant would have been the same as recited in claim 13 above. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Edwards047 with the art of Edwards065 to produce the claimed invention.

9. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are

representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Allowable Subject Matter

9.1. Claims 4, 5, 16 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9.2. The following is an examiner's statement of reasons for allowance:

9.2.1. While Edwards065 (Edwards U.S. Patent 6,918,065) and Edwards047 (U.S. Patent 6,530,047) both teach a method of exporting from a data processor emulation information including emulation control information and emulation data, none of these references taken either alone or in combination with the prior art of record disclose a method for exporting from a data processor emulation information having all of the claimed features of Applicant's instant invention, specifically including:

9.2.1.1. Regarding claim 4, "comparing respective sections of emulation data with the stored comparison data; and wherein the emulation control information in one of the information blocks includes a compression map indicative of whether the sections of the emulation data match the stored comparison data," in combination with the remaining elements and features of the claimed invention.

9.2.1.2. Regarding claim 5 "the method of claim 1 wherein the emulation data in one of the information blocks includes bits indicating whether the data processor performed data processing

operations during a corresponding clock cycle," in combination with the remaining elements and features of the claimed invention.

9.2.1.3. Regarding claim 16, "a comparator connected to said comparison data register and receiving emulation data generating an indication of a match between corresponding sections of said comparison data and said emulation data; and wherein the emulation control information in one of the information blocks includes a compression map indicative of whether the sections of the emulation data match the stored comparison data," in combination with the remaining elements and features of the claimed invention.

9.2.1.4. Regarding claim 17, "the method of claim 13 wherein the emulation data in one of the information blocks includes bits indicating whether the data processor performed data processing operations during a corresponding clock cycle," in combination with the remaining elements and features of the claimed invention.

9.3. It is for these reasons that the Applicant's invention defines over the prior art of record.

9.4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell L. Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 9:00 AM - 5:30 PM.
12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.
13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

Paul L. Rodriguez 12/6/05
Primary Examiner
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